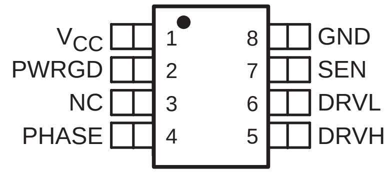
features

- DC-DC Synchronous Buck Controller
- Switching Frequency, 200 kHz (Typ)
- Programmable Output Voltage, 1 V to 2.5 V ±2%
- Power Good Function (PWRGD)
- Input Voltage, 12 V ±5%
- Drive High Load Current With External Components

SO (D) PACKAGE
(TOP VIEW)



NC − No internal connection

applications

- PC Motherboard, Voltage Regulation for System Power
- DDR Memory Supply (V_{DDQ} or V_{TT})
- RDRAM Memory Supply (V_{DDQ})
- General Purpose Synchronous Switch Mode Controller

description

The TPPM0115 is a synchronous buck controller capable of driving two external power FETs 180° out of phase. The device requires a minimum of external standard filter components and switching FETs to regulate the desired output voltage. This is achieved with an internal switching frequency of 200 kHz (typical).

The TPPM0115 switch mode controller and associated circuitry provide efficient voltage regulation of greater than 85%. The output voltage is set by two external resistors. During power up, when the output voltage reaches 90% of the desired value, the power good (PWRGD) output is transitioned high after a short delay of 1 ms to 5 ms. During power down, when the output voltage falls below 90% of the set value, the PWRGD output is pulled low without any delay.

In the event the set output is in an over-voltage condition due to a system fault, the drive to the lower FET turns on to correct the fault. There is a dead time between switching one FET ON while the other FET is switching OFF to prevent cross conduction.

The TPPM0115 is capable of driving high static load currents with minimal ripple on the output (<2%). The phase sense input is used to sense the flow of current through the inductor during flyback to minimize ripple on the output.

To optimize output filter capacitance, the voltage mode control is based on a fixed ON time during the start of the cycle and hysteretic control during load transients. This allows the device to respond and maintain the set regulation voltage.

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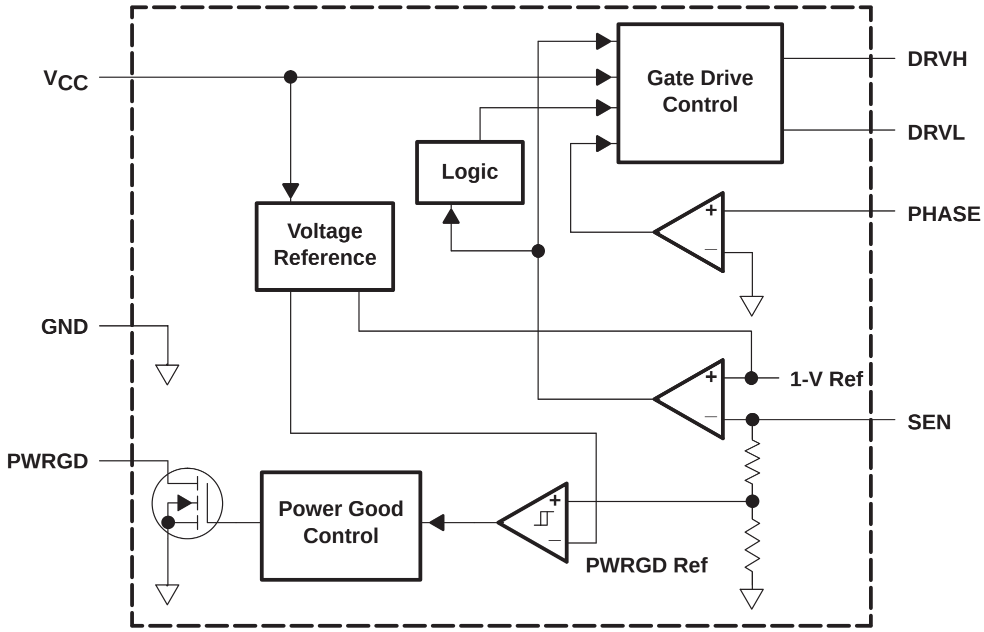
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DRVH	5	O	Output for upper FET gate drive
DRVL	6	O	Output for lower FET gate drive
GND	8	O	Ground
NC/TEST	3	O	No connection, used for test purpose only
PHASE	4	I	Phase sense input
PWRGD	2	O	Open-drain output for power good function
SEN	7	I	Sense input
V_{CC}	1	I	Input voltage

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Unregulated input voltage, V_{CC} (see Notes 1 and 2) . . . . 24 V
Drive output voltage, $V_{(DRVH)}$ and $V_{(DRVL)}$ (see Notes 1 and 3) . . . . 12.6 V
Power good voltage, $V_{(PWRGD)}$ (see Notes 1 and 2) . . . . 7 V
Feedback voltage, $V_{(SEN)}$ (see Notes 1 and 2) . . . . 7 V
Phase sense voltage, $V_{(PHASE)}$ (see Note 3) . . . . 7 V
Continuous power dissipation, P_D . . . . 0.4 W
Electrostatic discharge susceptibility, $V_{(HBMESD)}$ (see Note 4) . . . . 2 kV
Operating ambient temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature (soldering, 10 sec) T_{LEAD} . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Absolute negative voltage values on these terminals should not be below −0.5 V.
3. Absolute negative voltage values on these terminals should not be below −1 V.
4. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Unregulated input voltage, V_{CC}	11.4		12.6	V
Drive output current, $I_{(DRVH)}$ and $I_{(DRVL)}$		500		mA
Power good voltage, $V_{(PWRGD)}$		5		V
Feedback voltage, $V_{(SEN)}$		1		V
Phase sense voltage, $V_{(PHASE)}$		0		V
Continuous power dissipation, P_D		100		mW
Operating ambient temperature, T_A		55		°C

dc electrical characteristics, T_A = 0°C to 55°C, V_{CC} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	V_{CC} = 11.4 V to 12.6 V, I_L = 5 A to 10 A, See Figure 8 for external components, R_1 = 0, R_2 is not present		1			V
η	Efficiency	I_L = 10 A,	See Figure 8	86%			
I_Q	Quiescent current	$V_{(SEN)}$ = <1 V or >1.3 V, V_{OUT} = 1 V to 1.3 V			2		mA
$\Delta V_{O(\Delta IO)}$	Load regulation	See Figure 8		−1%		1%	
$\Delta V_{O(\Delta VI)}$	Line regulation						
	Temperature regulation						
$V_{OH(DRVH)}$	Upper drive output voltage	$V_{(SEN)}$ = 0.9 V,	I_{OH} = 200 mA		V_{CC}−3V		V
$V_{OL(DRVH)}$		$V_{(SEN)}$ = 1.2 V,	I_{OL} = −200 mA			1	
$V_{OH(DRVL)}$	Lower drive output voltage	$V_{(SEN)}$ = 1.2 V, $V_{(PHASE)}$ < 0 V	I_{OH} = 200 mA		5		V
$V_{OL(DRVL)}$		$V_{(SEN)}$ = 0.9 V,	I_{OL} = −200 mA			1	
I_{IH}	Phase input current	$V_{(SEN)}$ = 0.9 V,	$V_{(PHASE)}$ = 5 V		100		µA
I_{IL}		$V_{(SEN)}$ = 1.2 V,	$V_{(PHASE)}$ = −0.3 V		−50		
$V_{(PWRGD)}$	Sense output voltage for PWRGD detection range	Ramp up sense input until PWRGD transition to high		V_{OUT}* 0.86		V_{OUT}* 0.96	V
		Ramp down sense input until PWRGD transition to low		V_{OUT}* 0.63		V_{OUT}* 0.71	
I_{BIAS}	Sense feedback bias current	$V_{(SEN)}$ = 1.08 V				5	µA

ac electrical characteristics, T_A = 0°C to 55°C, V_{CC} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{sw}	Switching frequency	Measured at DRVH terminal			200		kHz
t_r	Output rise time for both DRVH and DRVL	$V_{(DRVH)}$ → 0 V to 8 V,	$V_{(SEN)}$ → 1.1 V to 0.9 V		50		ns
		$V_{(DRVL)}$ → 0 V to 8 V,	$V_{(SEN)}$ → 0.9 V to 1.1 V		50		
t_f	Output fall time for both DRVH and DRVL	$V_{(DRVH)}$ → 8 V to 0 V,	$V_{(SEN)}$ → 0.9 V to 1.1 V		50		ns
		$V_{(DRVL)}$ → 8 V to 0 V,	$V_{(SEN)}$ → 1.1 V to 0.9 V		50		
t_d	Power good signal delay	Delay time for $V_{(SEN)}$ > $V_{(PWRGD)}$ to PWRGD transitioning high		1		5	ms
t_{dt}	Dead time between DRVH and DRVL switch conduction	$V_{(SEN)}$ → 1.1 V to 0.9 V, Delay between $V_{(DRVL)}$ at 0 V and $V_{(DRVH)}$ = 1.5 V			50		ns
		$V_{(SEN)}$ → 0.9 V to 1.1 V, Delay between $V_{(DRVH)}$ at 0 V and $V_{(DRVL)}$ = 1.5 V			50		

thermal characteristics

		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal impedance, junction-to-case			50	°C/W
$R_{\theta JA}$	Thermal impedance, junction-to-ambient			178	°C/W

TYPICAL CHARACTERISTICS

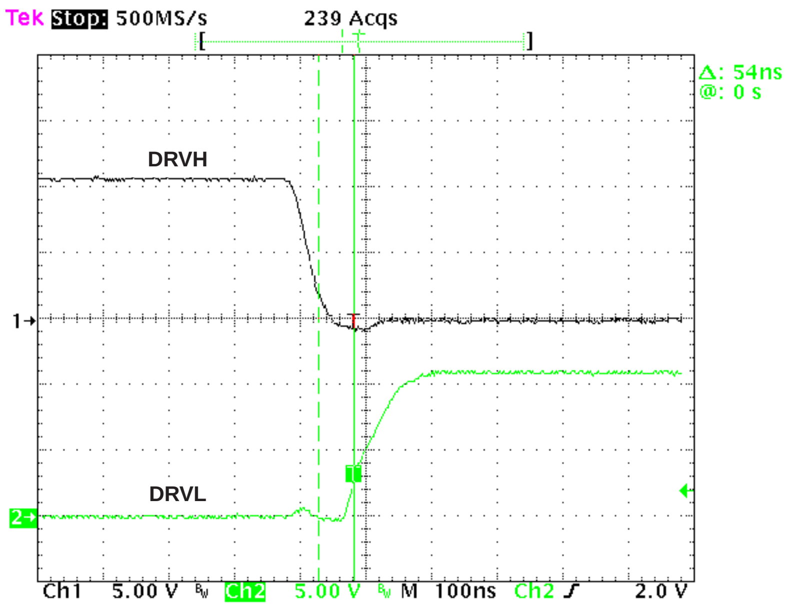


Figure 1. Dead Time Between Gate Drives Upper Switching OFF and Lower Switching ON

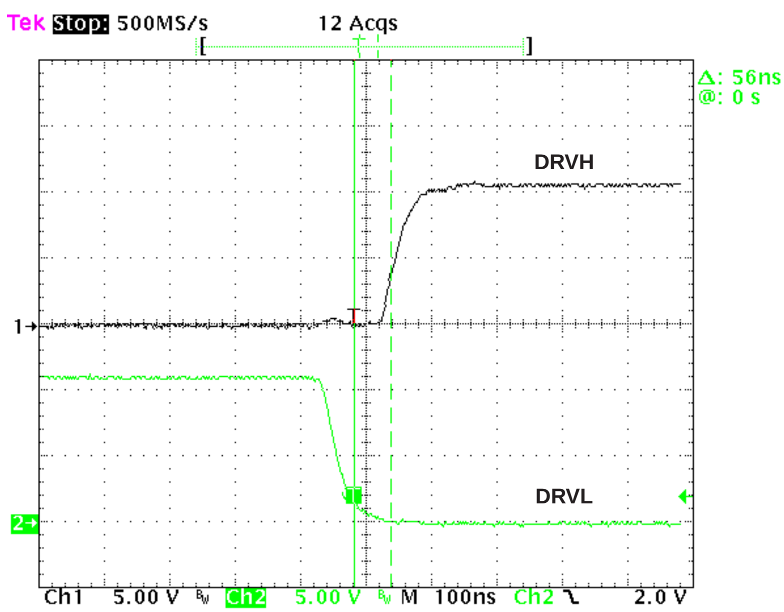


Figure 2. Dead Time Between Gate Drives Upper Switching ON and Lower Switching OFF

TYPICAL CHARACTERISTICS

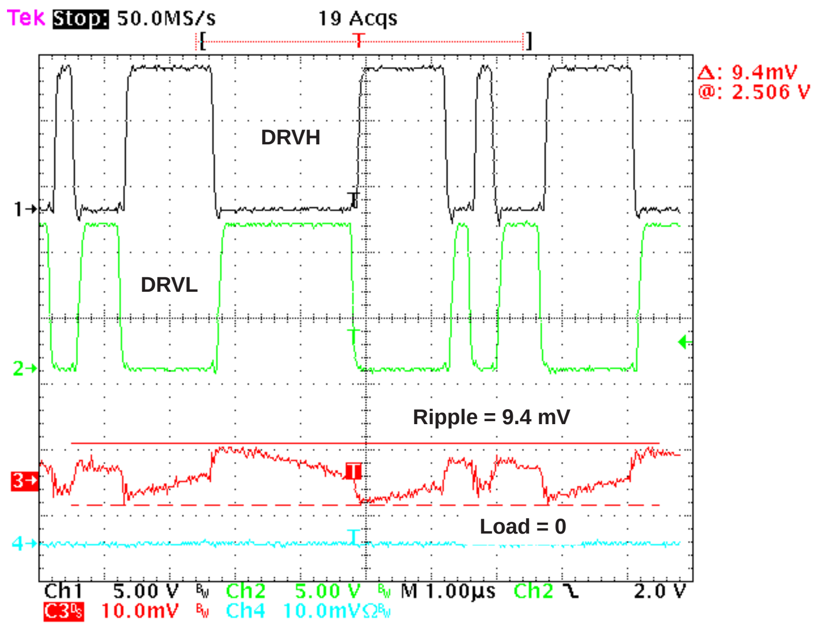


Figure 3. Output Voltage Ripple (Offset = 2.5 V) With NO Load

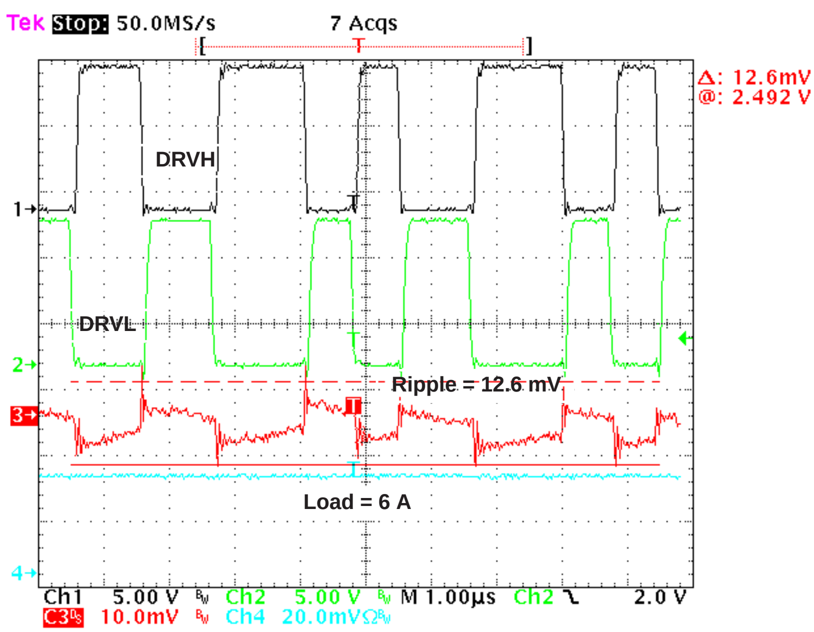


Figure 4. Output Voltage Ripple (Offset = 2.5 V) With 6 A Load

TYPICAL CHARACTERISTICS

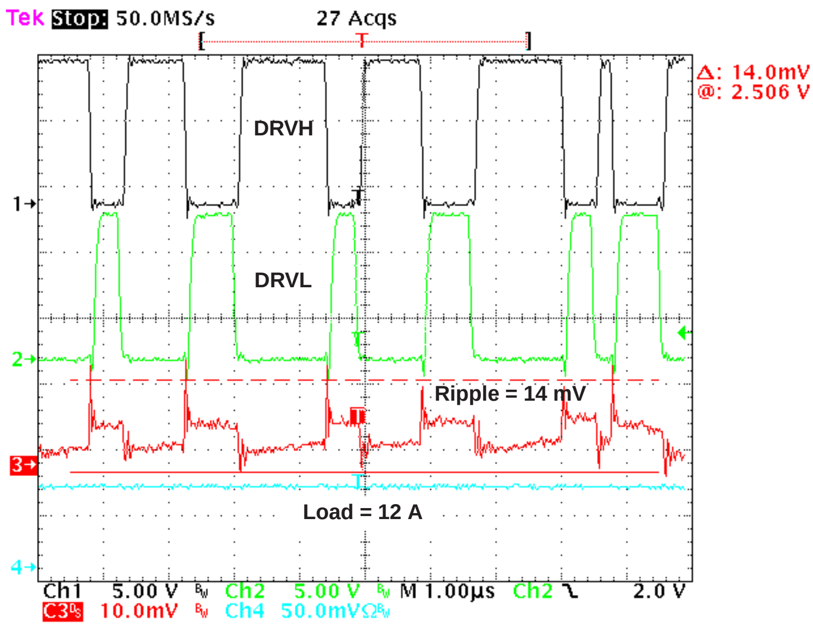


Figure 5. Output Voltage Ripple (Offset = 2.5 V) With 12 A Load

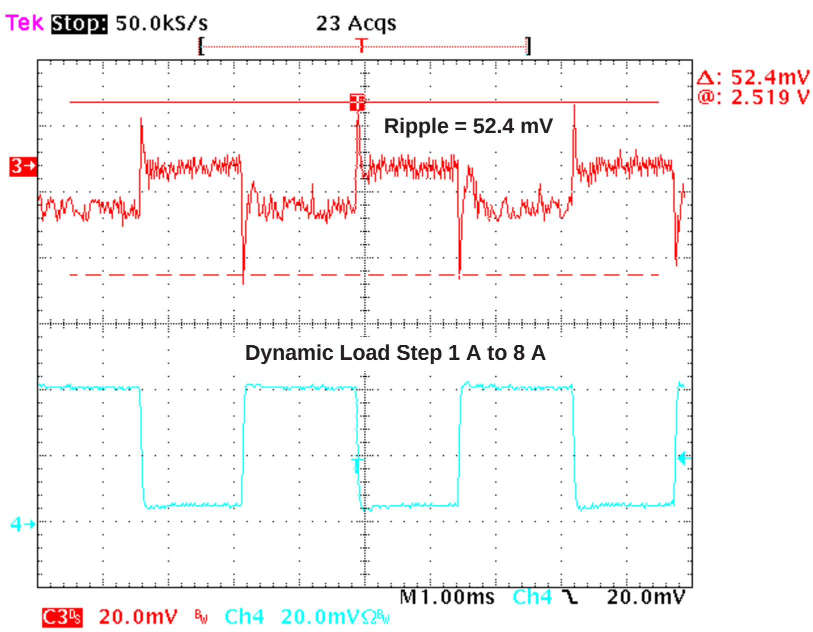


Figure 6. Output Voltage Ripple (Offset = 2.5 V) With Dynamic Load Switching (1 A to 8 A)

TYPICAL CHARACTERISTICS

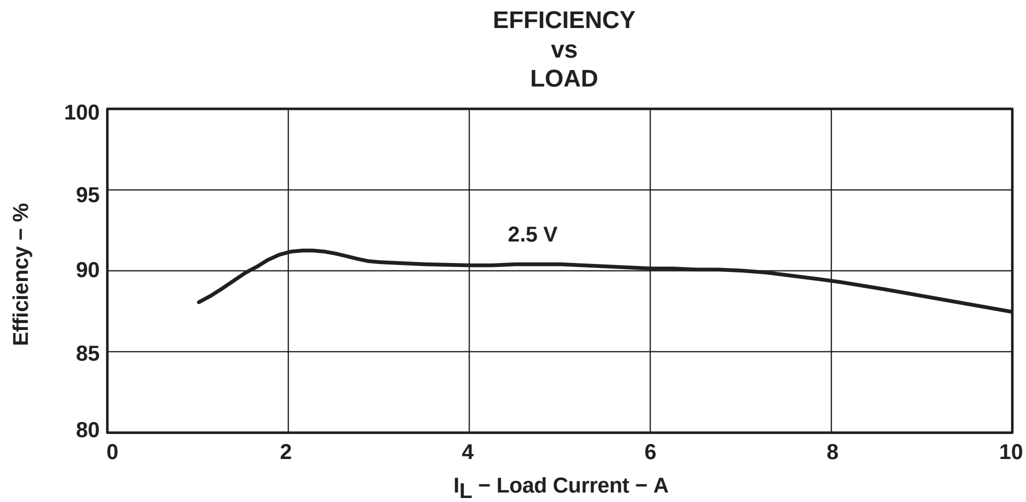
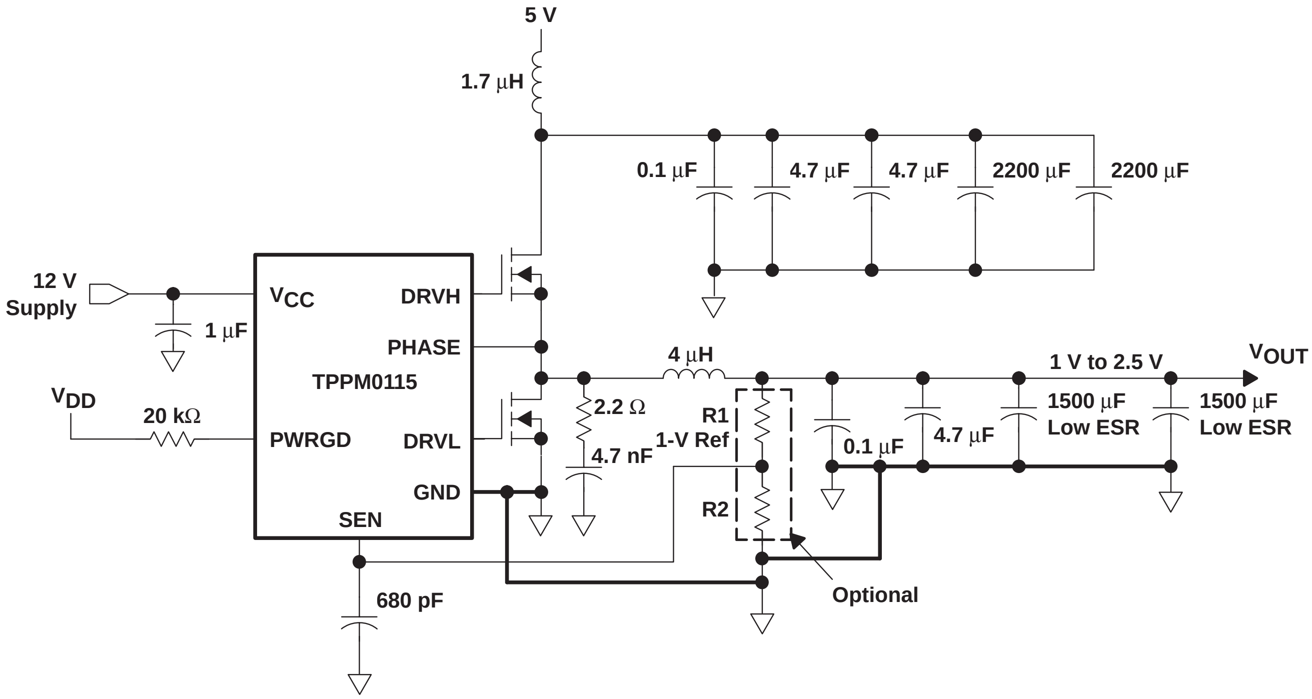


Figure 7. System Efficiency With Load Current (2.5-V Output)

APPLICATION INFORMATION



NOTES: A. The heavy lines must be kept short and connected to the ground plane construction for efficient results.
B. The feedback (sense) trace should be kept from the inductor flux.
C. The 1500-µF capacitor should have a low ESR to minimize output voltage ripple.
D. External FETs are MTD3302 or PHD55N03LT.
E. Set the resistor values on the SEN terminal using the following formulas:

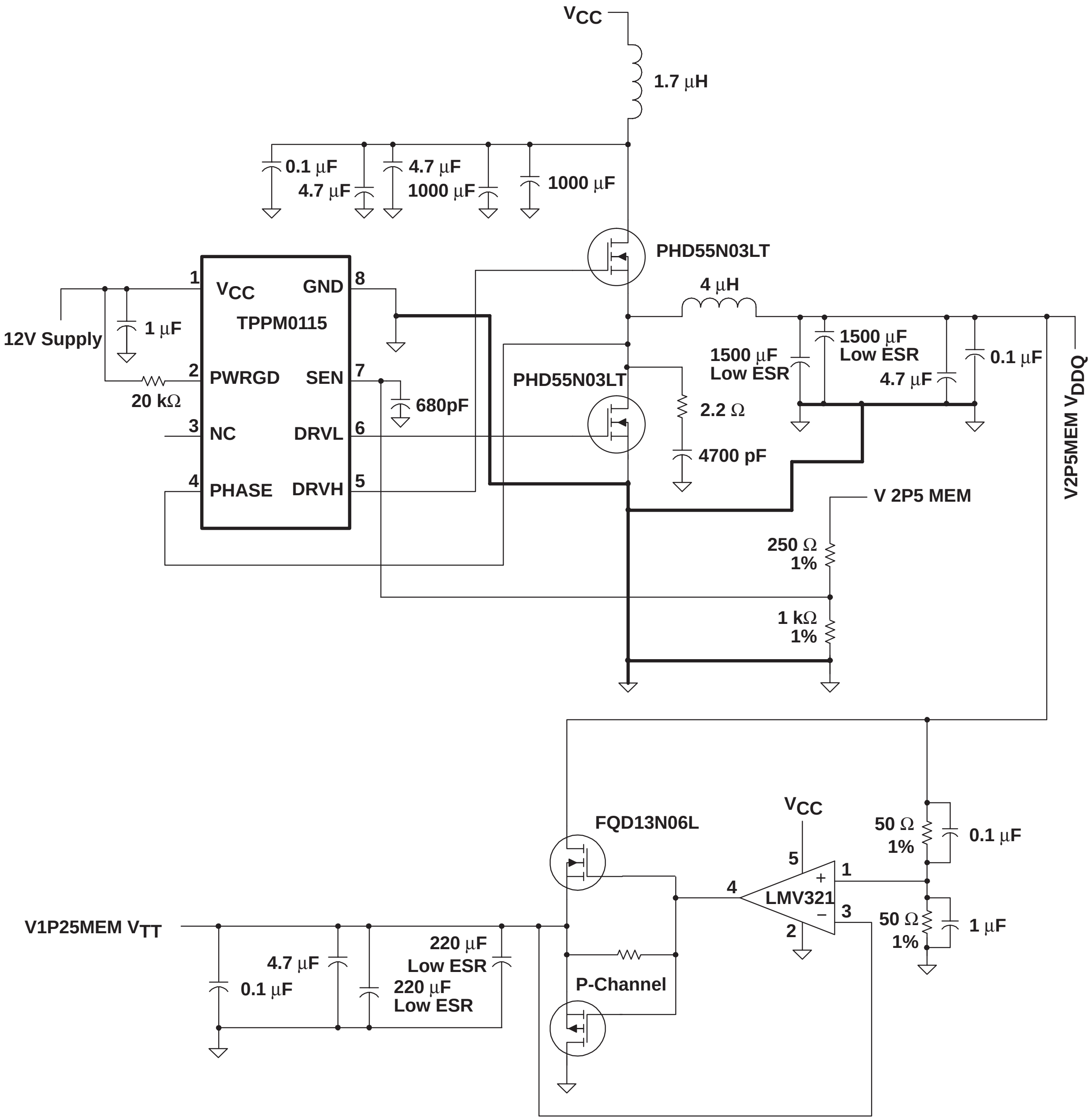
$$V_{OUT} = \frac{V_{ref}(R1 + R2)}{R2}, \quad \text{where } V_{ref} = 1\text{ V}$$

F. Maximum efficiency is dependent on proper selection of external components.
G. Line and load regulation is dependent on proper selection of external components.

Optional: When resistor feedback network is not used, V_{OUT} must be connected directly to SEN input to provide output regulation at $V_{OUT} = V_{ref}$.

Figure 8. Typical Application Schematic

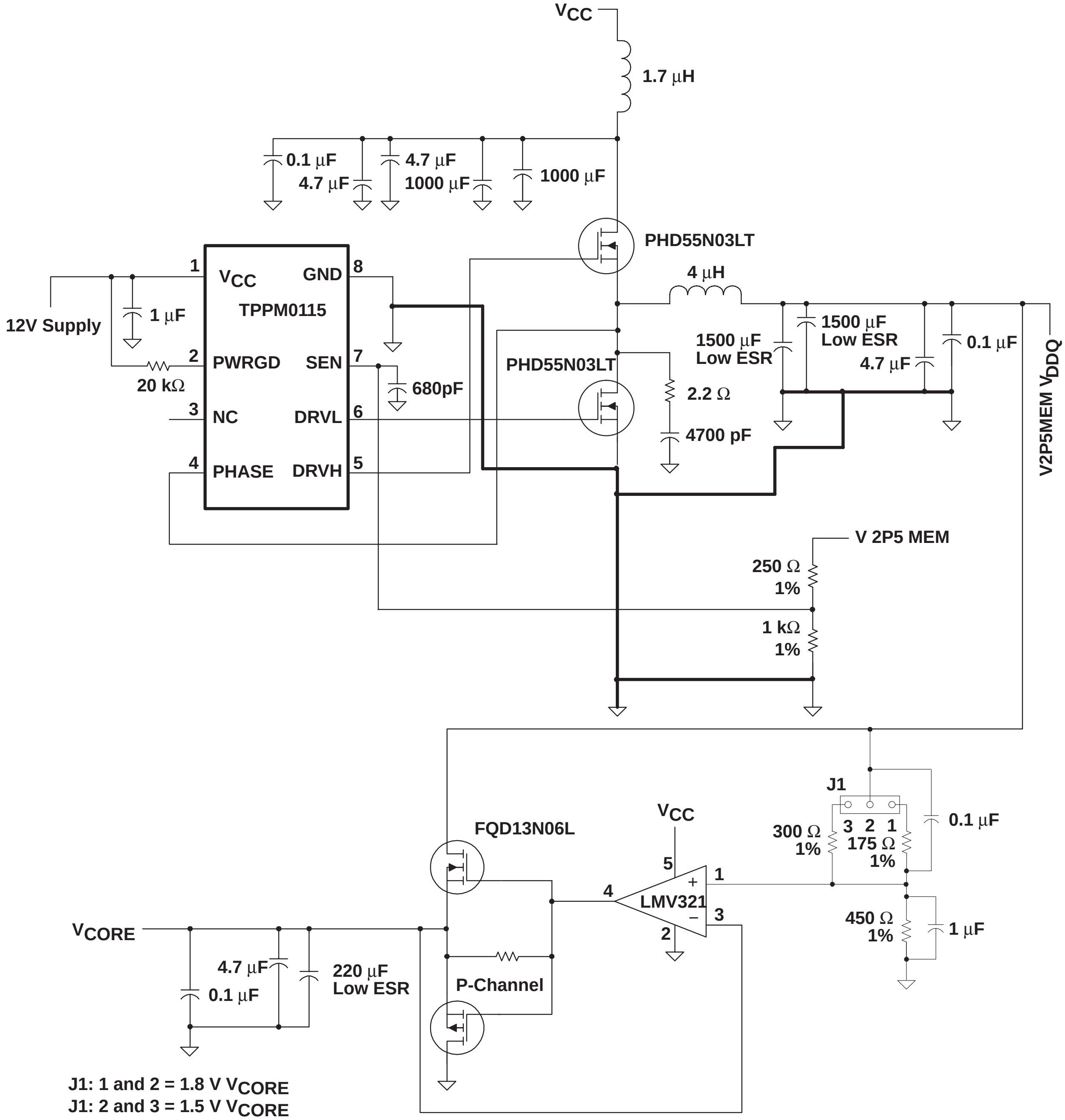
APPLICATION INFORMATION



NOTES: A. The heavy lines must be kept short and connected to the ground plane construction for efficient results.
B. The performance of the regulator depends on the proper selection of the external components for the application.

Figure 9. Application Schematic for DDR Memory V_{DDQ} and V_{TT} Supplies

APPLICATION INFORMATION



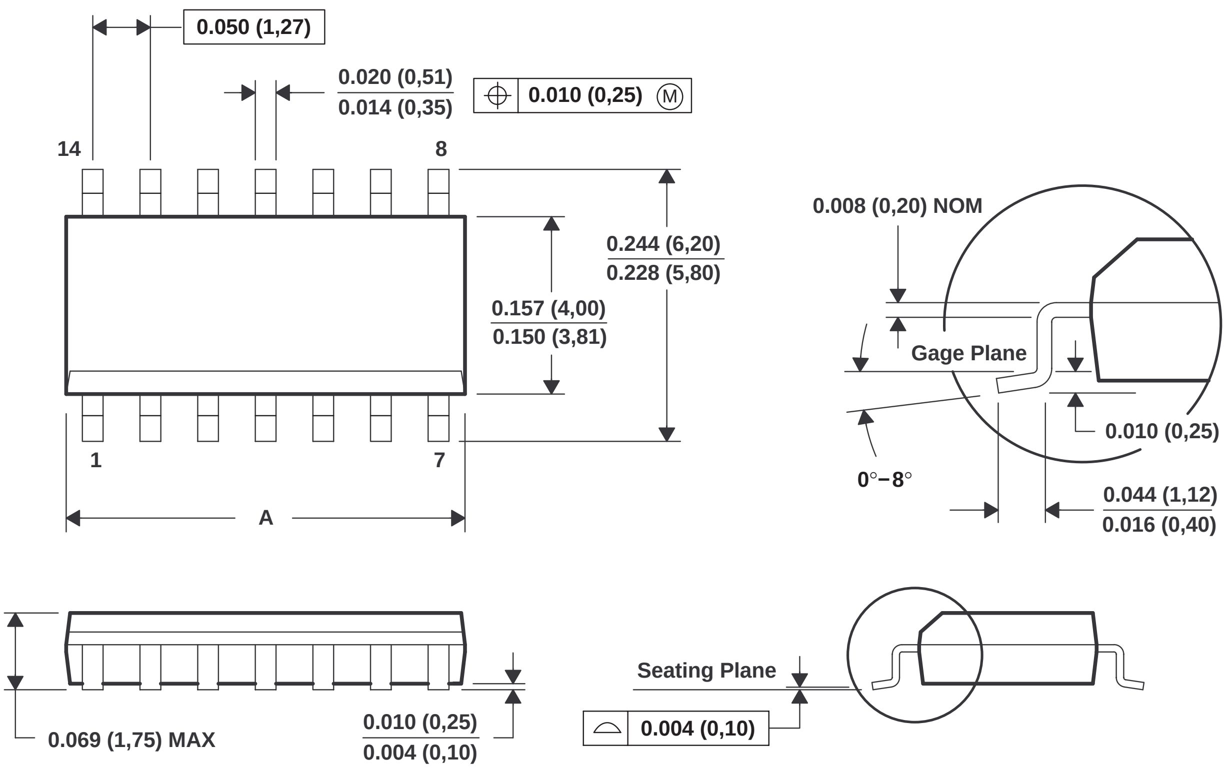
NOTES: A. The heavy lines must be kept short and connected to the ground plane construction for efficient results.
B. The performance of the regulator depends on the proper selection of the external components for the application.

Figure 10. Application Schematic for RAMBUS Memory V_{DDQ} and V_{CORE} Supplies

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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